IN THE SPECIFICATION:

Please amend the paragraph beginning on page 3, line 11, as follows:

FIG. 1A is a trellis diagram illustrating a number of primary vectors of a 5B/6B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 1B is a trellis diagram illustrating a number of primary vectors of a 5B/6B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 2 is a trellis diagram illustrating a primary vector of a 5B/6B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 3 is a trellis diagram illustrating a number of primary vectors of a 5B/6B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 4 is a trellis diagram illustrating a number of primary vectors of a 5B/6B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 5 is a coding table for the 5B/6B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 6 is a coding table for the 3B/4B-T code portion of an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 7 is a coding table for a basic set of control characters for an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 8 is a coding table for an additional set of control characters for an 8B/10B-T transmission code according to an embodiment of the invention;

FIG. 9A is a circuit diagram of the bit encoding portion of an 8B/10B-T encoder according to an embodiment of the invention;

FIG. 9B is a circuit diagram of the disparity control portion of an 8B/10B-T encoder according to an embodiment of the invention;

FIG. 9C illustrates the interrelationship between FIGS. 9B and 9B cont.;

FIG. 10 illustrates exemplary circuitry using the 8B/10B-T encoder shown in FIGS. 9A and 9B to compute disparity for a single byte through a faster implementation;

FIG. 11 illustrates exemplary circuitry using the 8B/10B-T encoder shown in FIGS. 9A and 9B to compute disparity for a single byte through a slower implementation;

FIG. 12 illustrates exemplary circuitry using the encoder shown in FIGS. 9A and 9B to compute disparity for four bytes through a faster implementation;

FIG. 12A illustrates the interrelationship between FIGS. 12 and 12 cont.;

FIG. 13 illustrates exemplary circuitry using the encoder shown in FIGS. 9A and 9B to compute disparity for four bytes through a slower implementation;

FIG. 13A illustrates the interrelationship between FIGS. 13 and 13 cont.;

FIG. 14 is a decoding table for decoding the 6B/5B-T code portion of a 10B/8B-T transmission code according to an embodiment of the invention;

FIG. 14A illustrates the interrelationship between FIGS. 14 and 14 cont.;

FIG. 15A is a circuit diagram of the decoding portion of a 6B/5B-T decoder according to an embodiment of the invention;

FIG. 15B is a circuit diagram of the disparity and error checking portion of a 6B/5B-T decoder according to an embodiment of the invention;

FIG. 16 is a decoding table for decoding the 4B/3B-T code portion of a 10B/8B-T transmission code according to an embodiment of the invention;

FIG. 17 is a circuit diagram of a 4B/3B-T decoder and error checks according to an embodiment of the invention;

FIG. 18 is a circuit diagram of a 10B/8B-T decoder using the 6B/5B-T decoder of FIGS. 15A and 15B and the 4B/3B-T decoder of FIG. 17;

FIGS. 19 and 20 illustrate exemplary circuitry using the 8B/10B-T decoder shown in FIG. 18 to compute disparity for a single byte through faster and slower, respectively, implementations;

FIG. 21 is a four-byte 10B/8B-T decoder;

FIG. 22 is a trellis diagram of a 10B/12B-T transmission code;

FIG. 23 is a table showing 5B/6B-T encoding for 10B/12B-T control characters;

FIG. 24 is a table of 6B trailers of the K3 vector used to form 12B control characters;

FIG. 25A is a circuit diagram for the 5B/6B-T portion of the bit encoding of a 10B/12B encoder;

FIG. 25B is a circuit diagram of the disparity control portion of the 10B/12B encoder;

FIG. 26A is a circuit diagram of the 6B/5B-T decoding portion of the 12B/10B decoding circuit; and

FIG. 26B is a circuit diagram of the disparity and error checking portion of the 12B/10B decoding circuit.